



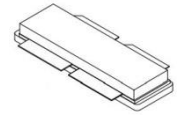
## 2400-2500MHz, 350W, High Power RF LDMOS FETs

### Description

The ITCH25350D4 is a 350-watt, internally matched LDMOS FETs, designed for Multiple use especially RF Energy application including cooking, heating and medical with frequencies from 2400 to 2500 MHz.

It is qualified up to 32V operation.

### ITCH25350D4



•Typical Performance (on Innogrations fixture with device soldered): Tcase=25 Degree C

Freq(MHz)	Pout (W)	Vdd(V)	Ids(A)	Gp (dB)	Eff(%)
2450	300	28	19.1	12.8	56.
2450	350	32	19.9	13.8	55
2450	400	32	22.4	12.4	55.8

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+32	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase= 85°C, Pout=350W CW	$R_{\theta JC}$	0.2	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DC Characteristics

Drain-Source Breakdown Voltage ( $V_{GS}=0V$ ; $I_D=100\mu A$ )	$V_{DSS}$	65	---	---	V
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Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ V}$ , $V_{GS} = 0\text{ V}$ )	$I_{DSS}$	---	---	10	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 6\text{ V}$ , $V_{DS} = 0\text{ V}$ )	$I_{GSS}$	---	---	1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 28\text{ V}$ , $I_D = 600\text{ uA}$ )	$V_{GS(th)}$	---	1.6	---	V
Gate Quiescent Voltage ( $V_{DD} = 32\text{ V}$ , $I_{DQ} = 20\text{ mA}$ , Measured in Functional Test)	$V_{GS(Q)}$		2.25		V

**Functional Tests (In Innegration Test Fixture, 50 ohm system) :**  $V_{DD} = 32\text{ Vdc}$ ,  $I_{DQ} = 20\text{ mA}$ ,  $f = 2450\text{ MHz}$ , CW Signal Measurements.,  $P_{in}=14.5\text{ W}$ ,

Power Gain	$G_p$	---	13.8	---	dB
Drain Efficiency@Pout	$\eta_D$	---	55	---	%
Output Power	$P_{-3dB}$	---	350	---	W
Input Return Loss	IRL	---	-7	---	dB

**Load Mismatch (In Innegration Test Fixture, 50 ohm system):**  $V_{DD} = 32\text{ Vdc}$ ,  $I_{DQ} = 20\text{ mA}$ ,  $f = 2450\text{ MHz}$

VSWR 10:1 at 350W pulse CW Output Power	No Device Degradation
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Figure 1

Signal: Pulse width 20us, duty cycle 10% ,  
Vgs= 2.26V,Vdd= 28V,I<sub>dq</sub>=20mA

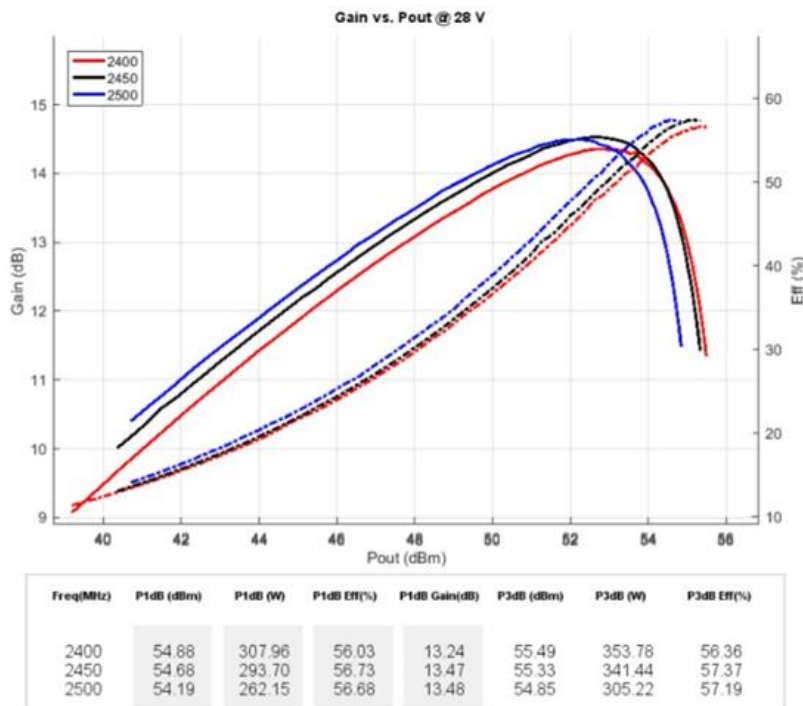


Figure 2

Signal: Pulse width20us, duty cycle 10%  
Vgs= 2.25V,Vds= 32V,I<sub>dq</sub>=20mA

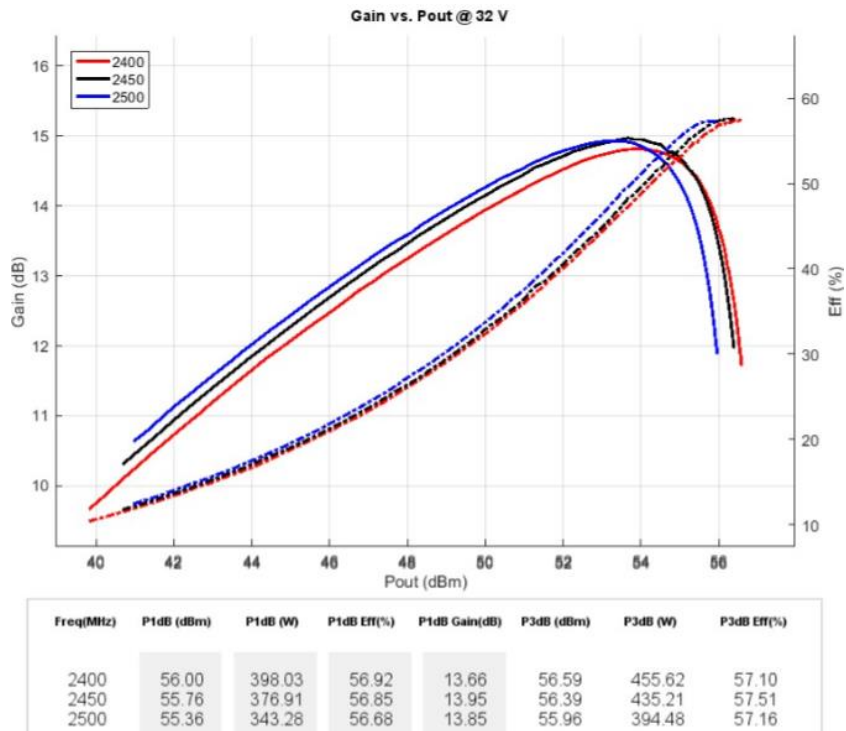


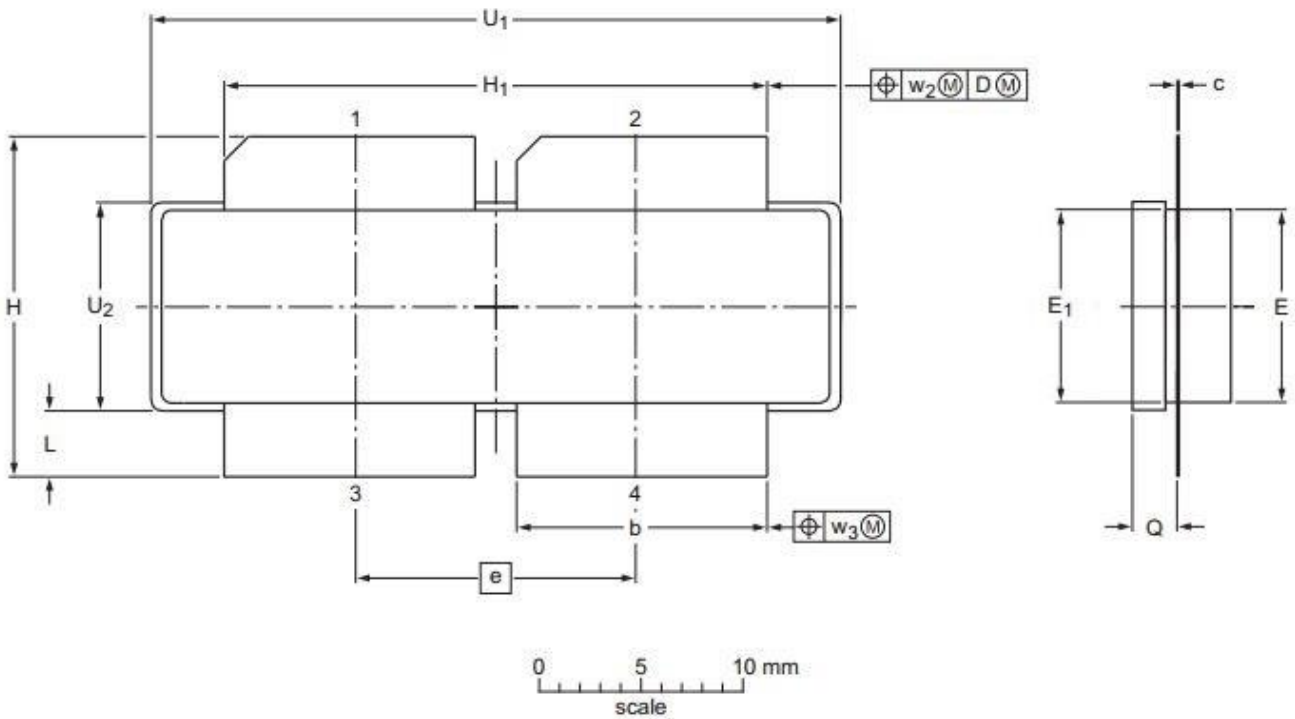
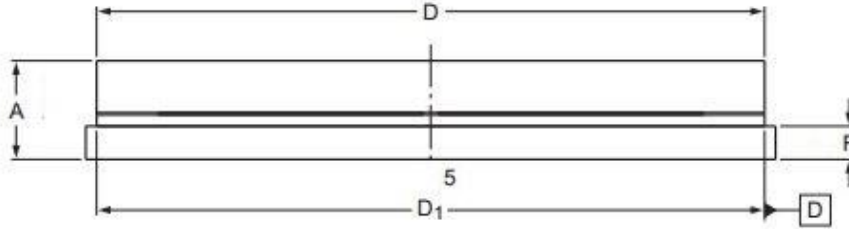
Figure3: Fixture circuit photo





### Package Outline

Earless flanged ceramic package; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/8/15	V1	Preliminary Datasheet Creation

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